



Chips, microelectronics, photonics

SNS-JU Hardware Technologies WG perspective

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New spectrum

- FR3 / cmWave
- mmWave & sub-THz
- Wider bandwidths
- New RF front-end requirements

AI-native networks

- Edge intelligence
- Hardware acceleration
- HW/SW co-design
- Energy-efficient processing

Integrated sensing

- Communication + sensing
- Full-/sub-band duplex operation
- New transceiver architectures
- RF sensing capabilities

Energy & sustainability

- Higher capacity within constrained power budgets
- Reduced RF-chain complexity
- Efficient devices and infrastructure
- Lifecycle considerations

The 6G system roadmap is increasingly constrained by what hardware can deliver efficiently, economically and at scale.

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6G systems, networks & services

- 6G architectures & use cases
- System-level KPIs and requirements
- RAN, NTN, ISAC, AI-native networks
- Integration, experimentation & validation

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System
/Technology
interface

Chips-JU

Semiconductor, photonic & integration technologies

- RF / analog / digital ICs & MMICs
- Photonics & optoelectronics
- Advanced semiconductor technologies
- Heterogeneous integration & packaging
- Design, prototyping & technology maturation

Chips for Europe Initiative

- Pilot Lines
- Design Platform
- Competence Centres

6G requirements & technology needs →

← Technology capabilities & constraints

RF / mmWave / sub-THz	FEM & antennas	Photonics	Compute & AI HW	Packaging & heterogeneous integration	Power & energy efficiency
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Shared hardware technology

Technology area	Technical scope	Example european players/projects
<u><i>RF front-end & transceivers</i></u>	RFIC/MMIC, PA/LNA, FEM, FR3, mmWave, D-/H-band, sub-THz	CEA-Leti — TERRAMETA; Nokia / STMicroelectronics / III-V Lab — X-TREME 6G
<u><i>Antennas & reconfigurable radio</i></u>	arrays, XL-MIMO, beamforming, RIS/metasurfaces, near-field	INESC TEC / CEA-Leti — TERRAMETA; CTTC / IMEC / CEA-Leti — 6G-REFERENCE
<u><i>Photonics & optical–wireless convergence</i></u>	integrated photonics, RoF/fronthaul, OWC, optical beamforming	AIT / Ligentec / III-V Lab — 6G-EWOC; PICadvanced — PROTEUS-6G / FLEX-SCALE
<u><i>Compute & signal processing HW</i></u>	DSP/PHY acceleration, RISC-V, edge AI, HW/SW co-design	University of Patras — X-TREME 6G; ETH Zürich — X-TREME 6G
<u><i>Integration & packaging</i></u>	heterogeneous integration, chiplets, AiP/AiM, interconnects, thermal	Fraunhofer IZM — X-TREME 6G; KIT / III-V Lab — X-TREME 6G

Common hardware challenges: Efficiency · bandwidth & linearity · integration · thermal management · manufacturability · test & validation

1. Multi-technology co-integration

CMOS/SiGe + III-V +
photonics + digital +
antennas

2. RF / package / antenna co-design

losses · parasitics ·
interconnects · AiP/AiM
· signal integrity

3. Power & thermal management

PA efficiency · compute
power · heat extraction ·
density

4. Calibration, control & reconfigurability

large arrays · RIS ·
beamforming · RF
impairments · sensing

5. Manufacturability & validation

yield · repeatability ·
mmWave/sub-THz
metrology · OTA

At 6G frequencies and integration densities, interfaces between technologies increasingly determine system performance.

TERRAMETA: integrated D-band radio + RIS

140–150 GHz D-band communication platform

- 45-nm CMOS RF front-end — CEA-Leti
- 40 × 40 transmissive RIS
- baseband + RF + RIS integration
- 57.6 Gb/s demonstrated in an earlier point-to-point configuration
- Industrial-robot demonstrator using an active RIS to overcome blockage

IC+RF

6G-EWOC: integrated photonics entering the radio architecture

Photonic technologies for 6G fronthaul & optical wireless

- chip-scale optical beamformer — AIT / Ligentec
- quasi-coherent optical transceiver technology
- fibre-wireless / optical-wireless integration
- connected mobility demonstrators

PIC+electronics

X-TREME 6G: packaging as part of the RF architecture

Heterogeneous integration for mmWave/sub-THz modules

- SiGe + GaN / InP technologies
- ultra-short RF interconnects
- advanced thermal management
- antenna/module integration
- Fraunhofer IZM packaging
- link to APECS Chips JU Pilot Line

Chips+package

1. RF front-end co-design

6G requirements -> semiconductor processes -> RFIC/FEM -> antennas/modules

2. mmWave / sub-THz hardware

devices, PAs, transceivers, packaging, antenna integration, test and validation

3. Heterogeneous integration

RF + digital + photonics + antennas + advanced packaging

4. Photonics for 6G

integrated photonics, optical/RF interfaces, fronthaul, distributed radio architectures

5. Joint validation

common reference specifications, measurement methodologies, demonstrators and cross-region experimental validation

6G SNS

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